PROCEDURE IV: forming the backside p^+ emitter with a required thickness by ion implanting into the surface of the residual diffused-layer;

PROCEDURE V: depositing metals on the surface of the backside p^+ layer, followed by sintering/alloying; and

after the substrate is thinned, i.e. after PROCEDURE III or since PROCEDURE IV, only low-temperature processes occur.

7. The method as defined in claim 6, wherein said low temperature is considered to be less than 600 °C.

REMARKS

This Amendment is submitted in response to the Office Action mailed on June 14, 2002 in which claims 1-7 were pending. The Office Action included a restriction requirement between Group I, a semiconductor device represented by claims 1-5, and Group II, a method of manufacturing a semiconductor device, represented by claims 6 and 7. With this Amendment, Applicant traverses the restriction requirement, while electing the invention of Group II.

Applicant traverses the restriction requirement because the apparatus claims and the method claims are not distinct. The method required by claims 6 and 7 is specially designed to produce the semiconductor device of Group I. The method is sufficiently detailed so as to produce the desired semiconductor device, and not some other, materially different product. The Examiner justified the restriction requirement by stating:

> For example, the process of claim 6 can be materially altered by forming a nonuniformly doped n-type substrate which contains a diffused n+ layer on one side wherein the diffused layer, which is near to the backside p+ emitter (sic) into the surface of residual diffused layer, then forming the wafer from the high concentration side of the substrate by such commonly used techniques as grinding and polishing, then forming the general front side structure of either

> IGBT, MCT, or GTO on the low concentration side of the n-type substrate using ion implanting, high temperature diffusion.

(Office Action, p. 2). Applicant respectfully submits that the above-described process would not reliably produce the claimed product because it thins the wafer through grinding and polishing prior to forming the high-temperature front-side, increasing the probability of breakage during the high-temperature process.

The wafer thickness of 100-200 μm is the final thickness, and not the thickness during most of the process steps, especially the high-temperature (such as greater than 600 degrees Celsius and up to more than 1000 degrees Celsius) steps for producing the front-side structure of the device. Wafers of 100-200 μm thickness tend to break during the high-temperature processing steps. Moreover, mechanical actions on such a thin wafer at lower temperatures also increase the probability of breakage. Wafer thinning from 300-400 μm or more to 100-200 μm is feasible only in the last few processing steps at lower temperature.

The alleged procedure provided by the Examiner as justification for the election requirement cannot be used to produce the invention, as defined in the claims, because th Examiner's alleged procedure would thin the wafer to a fragile thickness before the high-temperature, front-side making steps. Such a process would more likely than not result in breakage during the high-temperature steps or later in mechanical processing steps at lower temperature.

Moreover, it is not at all clear that the semiconductor device of Group 1 can be produced by another process that is materially different from the method required by claims 6 and 7. As mentioned in the application, the product and process are oriented to power devices with voltage ratings under 2 kV. (See page 4, line 18). While other processes have been used to produce semiconductor devices with voltage ratings under 2 kV, prior art low-voltage IGBT wafers with an n-substrate thickness of only approximately 100-200 μm typically experience cracking during the multi-step high-temperature processes. (see p. 3, line 9).

The proposed thickness for the n-type buffer layer (or residual diffused-layer) is more than 5 μm. Such a thickness can be easily achieved by diffusion, but not easily and practically by

ion implantation without a high-temperature annealing/drive-in process. As described in the application, ion implantation produces a thinner backside p+ emitter with lower doping concentration, and thus results in larger electron current flow through the emitter. This ion implanted emitter provides a smooth path for the excess electrons stored in the n-type base to be drawn out during turn-off, so that switching time is shorter.

Diffusion or ion implanting with high-temperature drive-in to form the 5 μm thick backside n buffer layer after producing the front-side structure, but before the wafer thinning process, will severely effect the junction depths of the front-side structure. In particular, submicron junctions will be impacted, making this arrangement very impractical. Diffusion or ion implanting with high-temperature drive-in to form the 5 μm thick backside n buffer layer and/or the backside p+ emitter, after thinning of the wafer to 100-200 μm, also increases the likelihood of breakage.

While it may be possible to use double deep in diffusion of both n+ and p+ into the starting substrate and thin the wafer in the last process step to achieve the semiconductor device of Group I, it is not practical for two reasons: 1) it is difficult to control the size of the p+ emitter during the wafer thinning process; and 2) the p+ layer cannot be easily adjusted. First, claim 1 requires "an ultra thin and lightly-doped backside p^+ emitter". It is difficult to control the size of the p+ emitter during thinning. Additionally, the residual concentration of the residual deep-diffused (several tens or 100-200 μm) p+ layer cannot be easily adjusted. By contrast, the p+ dose implanted into the backside is very convenient to control according to different on-voltage and switching time requirements (see claim 3).

Accordingly, the method of claims 6 and 7 provides the only practical way to produce the product of claims 1-5. Thus, the product and the method are not distinct. Nevertheless, Applicant, with traverse, elects the Group II invention of the method of manufacturing a semiconductor device as represented by claims 6 and 7. Claims 2-5 have been amended to define method details and to depend from method claim 6.

All of pending claims 1-7 are in condition for allowance. Reconsideration and notice to that effect is respectfully requested. The Examiner is invited to contact the undersigned attorney at the telephone number listed below if such a call would in anyway facilitate the prosecution of this application.

Respectfully submitted,

KINNEY & LANGE, P.A.

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